



USING COCOTB AS A VERIFICATION FRAMEWORK FOR HDL DESIGNS

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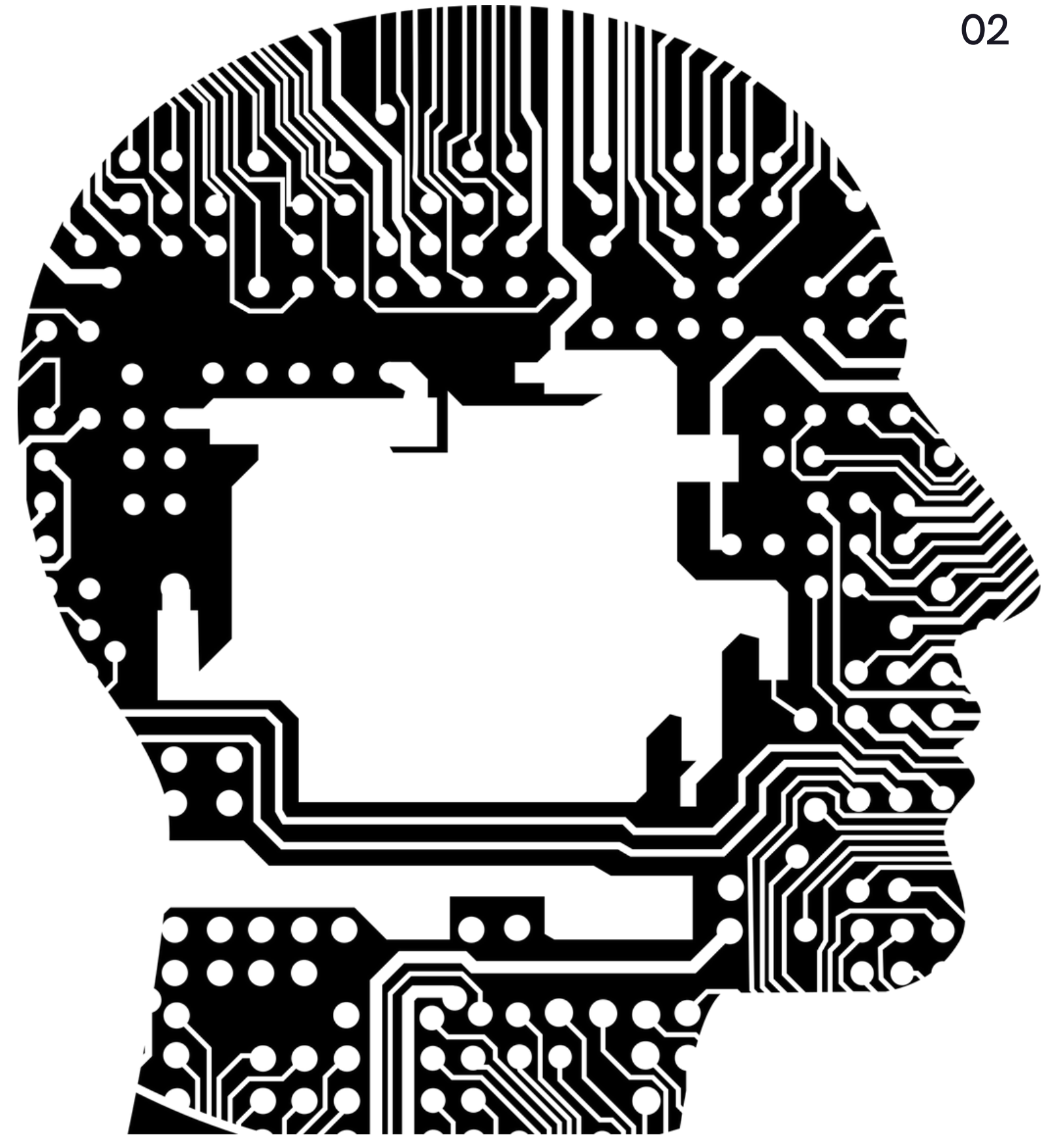
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Introduction

What is the project about

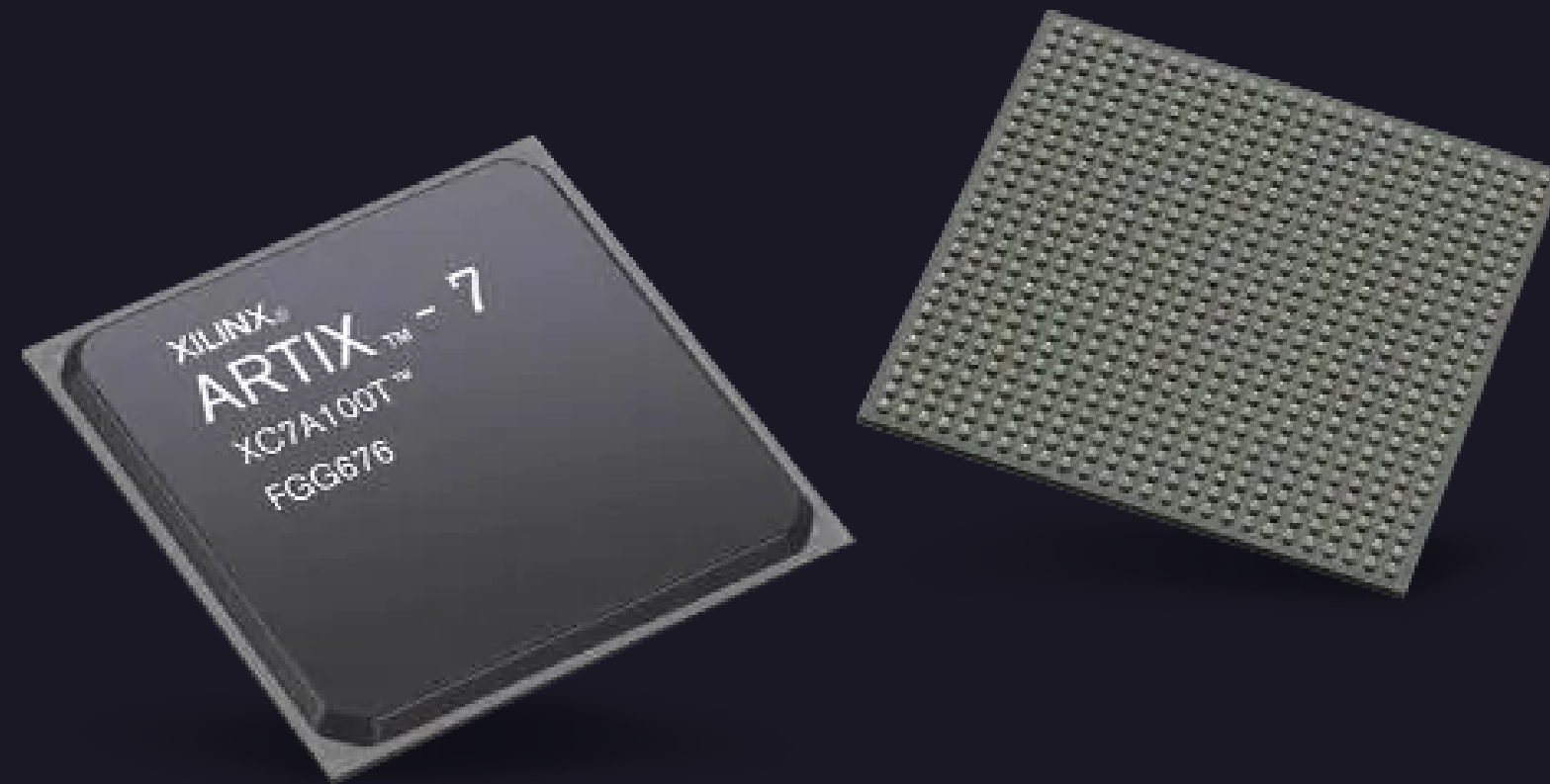
What were my tasks

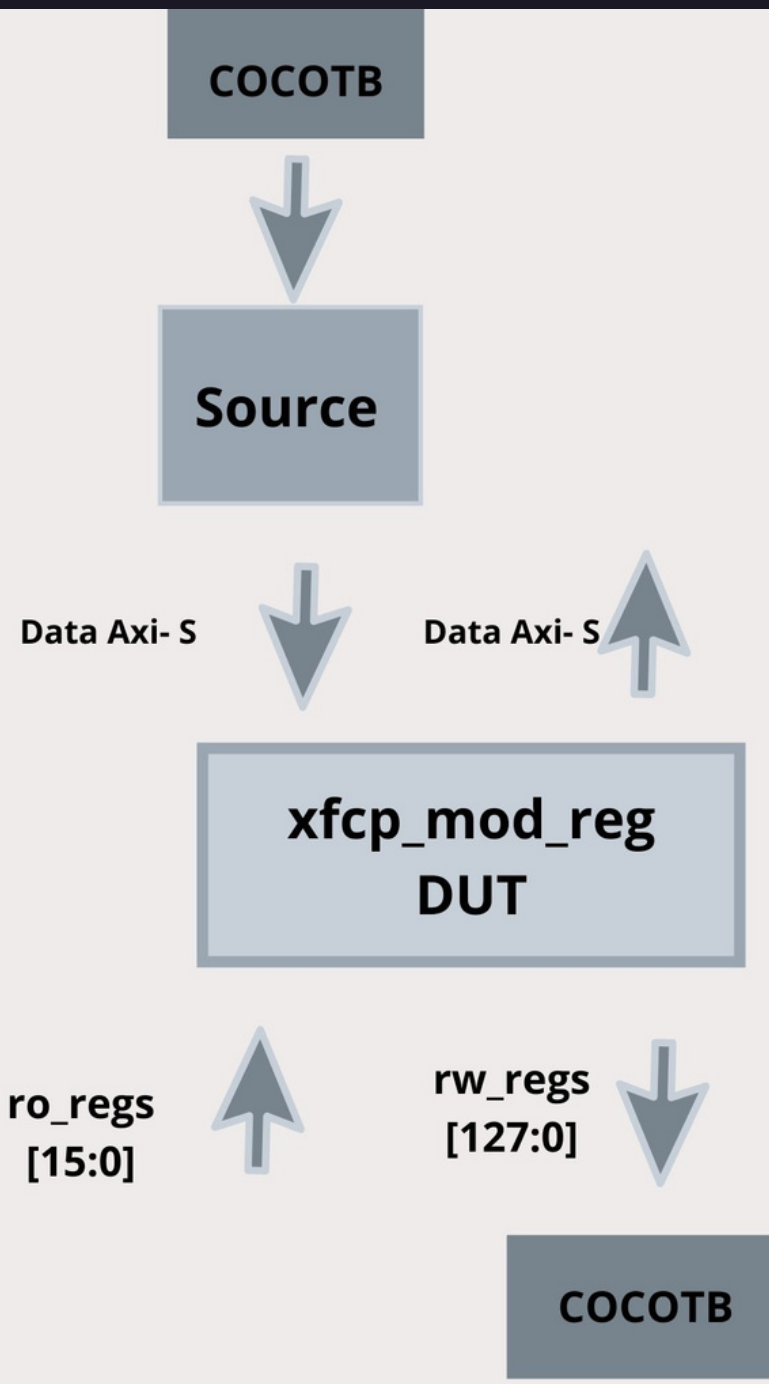
02



FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence the term "field-programmable".





Write register requests

- offset
- data

```
test_xfcp.py > xfcp_prep
1 | import bitarray
2 | import math
3 | import os
4 | import random as rnd
5 | from collections import Counter
6 | from typing import Dict, List, Any
7 | from cocotb.axi import AxiStreamFrame, AxiStreamBus, AxiStreamSource, AxiStreamSink, AxiStreamMonitor
8 | import cocotb
9 | from cocotb.binary import BinaryValue
10 | from cocotb.clock import Clock
11 | from cocotb.triggers import RisingEdge, FallingEdge
12 | from cocotb.queue import Queue
13 | from cocotb.handle import SimHandleBase
14 | from cocotb.triggers import Event
15 | from dose3d_daq.xfcp_ext import reg_packet
16 |
17 |
18 | @cocotb.test()
19 | async def xfcp_prep(dut):
20 |     #wygenerowanie clocka:
21 |
22 |     clock = Clock(dut.clk, 8, units="ns") # Create a 10us period clock on port clk
23 |     cocotb.fork(clock.start()) # Start the clock
24 |
25 |     # Reset DUT
26 |     await FallingEdge(dut.clk)
27 |     dut.rst <= 1
28 |     dut.rw_set <= 0
29 |     dut.rw_rst <= 0
30 |     for _ in range(3):
31 |         await RisingEdge(dut.clk)
32 |     dut.rst<= 0
33 |
34 |     source = AxiStreamSource(AxiStreamBus.from_prefix(dut, "up_xfcp_in"), dut.clk, dut.rst)
35 |
36 |     for _ in range(10):
37 |         await RisingEdge(dut.clk)
38 |
```

```
test_xfcp.py > xfcp_prep
36     for _ in range(10):
37         await RisingEdge(dut.clk)
38
39
40
41
42     for i in range(16):
43         pkt = reg_packet.WriteRegisterRequest()
44         pkt.data = bytearray([rnd.randint(0, 255) for _ in range(16 - i)])
45         pkt.offset = i
46         test_data = pkt.build()
47         test_frame = AxiStreamFrame(test_data, tx_complete=Event())
48         await source.send(test_frame)
49         await test_frame.tx_complete.wait()
50         await RisingEdge(dut.clk)
51         await RisingEdge(dut.clk)
52
53         #print(pkt.data)
54         #print(pkt.offset)
55         #print(dut.rw_regs.value.binstr)
56         s=dut.rw_regs.value.binstr
57         check = bytearray()
58         for a in range(16):
59             c= s[a*8:(a+1)*8]
60             n= int(c, 2)
61             check.append(n)
62         check=check[::-1]
63         #print(check)
64         assert pkt.data==check[pkt.offset:]
65
66
67         if pkt.data==test_data:
68             assert True
69
70     for _ in range(10):
71         await RisingEdge(dut.clk)
72
```


File Edit Search Time Markers View Help

From: 0 sec To: 3704001 ps Marker: 468900 ps Cursor: 533100 ps

C:\Users\krolm\Desktop\ss\cocotb\dump.vcd C:\Users\krolm\Desktop\ss\cocotb\dump.vcd C:\Users\krolm\Desktop\ss\cocotb\dump.vcd C:\Users\krolm\cocotb\examples\adder\tests\dump.vcd C:\Users\krolm\Desktop\ss\cocotb\dump.vcd

SST

- xfcp_mod_req

Time

```
clk=0
rst=0

up_xfcp_in_tdata[7:0]=01 32 00 01 00 48 B6 D7 AD E8 D1 F2 56 2F 2B D6 88 FF 71 A0 FF 32 00 01 00 01 00
up_xfcp_in_tlast=0
up_xfcp_in_tready=1
up_xfcp_in_tuser=0
up_xfcp_in_tvalid=1

up_xfcp_out_tdata[7:0]=00
up_xfcp_out_tlast=0
up_xfcp_out_tready=z
up_xfcp_out_tuser=0
up_xfcp_out_tvalid=0

rw_regs[127:0]=A0 00000000000000000000000000000000 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ 0+ A071FF88D62B2F2F56F2D1E8ADD7B648
```

Type	Signals
reg	regs_read_ptr_reg[
wire	regs_reserved[63:0]
reg	regs_write_ptr_reg[
reg	regs_write_ptr_reg_
wire	ro_regs[15:0]
reg	ro_regs_freeze
reg	ro_regs_reg[15:0]
wire	rst
wire	rw_regs[127:0]
reg	rw_regs_reg[127:0]
reg	rw_regs_reg_next[1
wire	rw_rst[127:0]
wire	rw_set[127:0]
reg	rx_state_next[3:0]
reg	rx_state_reg[3:0]

Filter:

Append Insert Replace

Waves

